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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,624	06/30/2000	Stephen Jourdan	2207/8609	9451

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EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/608,624	JOURDAN ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/13/06* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-20,23-30 and 38-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-20,23-30 and 38-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Appeal Brief

1. In view of the Supplemental Appeal Brief filed on 1/13/06, PROSECUTION IS HEREBY REOPENED. The Office Action with the new ground(s) of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-3, 9-15, 20, 23-30, and 38-43 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims to computer-related inventions that are clearly nonstatutory fall into the same general categories as nonstatutory claims in other arts, namely natural phenomena such as magnetism, and abstract ideas or laws of nature which constitute "descriptive material. "Abstract ideas, Warmerdam, 33 F.3d at 1360, 31 USPQ2d at 1759, or the mere manipulation of abstract ideas, Schrader, 22 F.3d at 292-93, 30 USPQ2d at 1457-58, are not patentable. Descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).) "Nonfunctional descriptive material" includes but is not limited to music, literary works and a compilation or mere arrangement of data (See MPEP section 2106, IV, B, 1).

Note as to claim 1, the essential element of the claimed invention, *"a memory entry storing a trace"* is descriptive material per se and is non-statutory because it is not capable of, by itself, causing functional change in the computer. Note a *trace* comprises the sequences of executed instructions (see page 1, lines 16 in the specification for the definition of "trace"), e.g., it comprises the address data (or pointers) of executed instructions (see page 473 of the attached Microsoft Computer Dictionary, 5th edition for the definition of "sequence"). Further, in claim 1, line 2, "having a multi-entry, single exit architecture" is just an alternative pattern of the data saved in the trace. A data is a data. Data **per se**

is non-statutory. Similar problems exist in claims 2, 3, 20, 23-27, and 38-43. Further note, in claims 23, and 41-43, "means for indexing the trace", e.g. index bit, is the additional data added to the trace. The limitation does not make the claims statutory. If Appellant is alleging that the "multiple-entry, single exit architecture" of the stored trace constitutes a data structure and not data, per se, Appellant needs to show how it meets the IEEE definition of a data structure, namely, "a physical or logical relationship among data elements, designed to support specific data manipulation functions."

Claim 9 comprises steps of receiving, assembling, and determining. They are just an abstract idea. The claim does not provide practical application that produces a useful, tangible and concrete result. Therefore, this claim is non-statutory. Note the step of selecting is nothing more than a thought or a computation within a processor, both of which are abstract and not a real world result. It's not until what is selected is used or at least made available for use that it reasonably becomes a practical application of the idea. Additionally, the method is silent as to what occurs if there is no match, leaving the method at the determining step. Once again, merely determining is just a thought or a computation within a processor and does not appear to produce a tangible result.

Claims 10 and 15 appear to each only resolve one of these deficiencies, but it is not believed either resolves both of them. Similar problems exist in the other claims 11-14.

Regarding Claim 28, as set forth above, a trace is a sequence of executed instructions (see Page 1, lines 16 of the specification). It comprises such as address data of the executed instructions. Data per se is non-statutory. Therefore, this claim is non-statutory. Even if it is somehow determined to be functional descriptive material, they're then just functional descriptive material, per se. Merely claiming functional descriptive material does not make it statutory. Similar problems exist in claims 29 and 30.

Claim Objections

4. Claim 15 is objected to because of the following informalities:

in claim 15, line 2, it is suggested to insert -extended- after "selected".

Appropriate correction is required.

5. Claim 39 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the

claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Note in claim 38, line 3, that what it is intended "to store" is immaterial. Therefore, in claim 39, "a trace is a complex trace having multiple independent prefixs and a common, shared suffix" to be stored is immaterial and the claim fails to further limit the subject matter of claim 38.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 23-27, and 41-43 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the

inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 23, and 41-43 recited indexing means, however, in the specification there's no description about the structure for the indexing means necessary for supporting the claims.

Appropriate correction is required.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-3, 4-7, 20, 23-30, and 41-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, an "entry" is, according to IEEE definition (see also page 195 of the attached Microsoft Computer Dictionary, 5th edition), nothing more than *a unit of information*. Thus, it is not clear how claim 1 constitutes an apparatus and how a memory entry can store anything. Instead, in accordance with it's normal and ordinary meaning a memory

entry can be itself stored in memory, and no memory is claimed as part of the so-called apparatus.

In claim 1, it is not clear how a "trace" can have a multi-entry and single exit. Note a trace comprises the sequences of executed instructions (see page 1, lines 16 in the specification), e.g. it comprises the address data (or pointers) of executed instructions. Note a trace is a sequence of program instructions. The flow of a program can only have one entry in a trace (see the attached reference of Nair Ravi, " Trace Caches and Trace Processors", lecture note, Pages 1-2, USPTO training for examiners in the computer architecture area, 4/29/04) since the trace is dependent on the input to the program. A trace is not a program. Some essential elements are missing. Similar problems exist in claim 38. Note the complex block as shown in Fig. 6 is the combination of two independent blocks (traces), XBold and XBnew. XBold or XBnew can have only one entry IP2 or IP4. While Applicants can be their own lexicographer, they cannot attribute a meaning repugnant to its normal and ordinary meaning in the art.

In claim 3, it is not clear what is meant by "terminal instruction therein". It appears that the terminal instruction is inside a trace stored in the memory entry. However, a trace comprises the sequences of executed instructions (see page 1,

lines 16 in the specification), e.g. it comprises the address data (or pointers) of executed instructions. The address data is not an instruction. Therefore, a trace does not have a terminal instruction therein. Similar problems exist in the other claim 30, and 40.

In claim 4, lines 6 and 7, it is not clear how to define "complex blocks" and "block prefixes" since the structural relationship between "complex blocks", "block prefixes", and the front-end system was not defined.

In claim 6, it is not clear what is meant by "blocks having a multiple-entry, single exit architecture". Some essential elements or more detailed descriptions are missing. Similar problems exist in claim 38. Note the complex block as shown in Fig. 6 is the combination of two independent blocks (traces), XBold and XBnew. XBold or XBnew can have only one entry IP2 or IP4. Similar problems exist in claims 16, and 17.

In claim 20, line 3, it is not clear what is meant by "a last instruction in the memory entry". It appears that the last instruction is inside a trace stored in the memory entry based on lines 1-2 about a trace. However, a trace comprises the sequences of executed instructions (see also page 1, lines 16 in the specification), e.g. it comprises the address data (or pointers) of executed instructions. The address data is not an

instruction. Therefore, a trace does not have a last instruction therein and the memory entry does not have the last instruction, either. Similar problems exist in claims 22-24, and 41-43.

In claim 20, lines 3-4, it is not clear how a trace has multiple separate prefixes. As set forth above, a trace is a sequence of program instructions. The flow of a program can only have one entry in a trace (see the attached reference of Nair Ravi, " Trace Caches and Trace Processors", lecture note, Pages 1-2, USPTO training for examiners in the computer architecture area, 4/29/04) since the trace is dependent on the input to the program. Note the complex block as shown in Fig. 6 is the combination of two independent blocks (or traces) , XBold and XBnew. XBold or XBnew can have only one entry IP2 or IP4. Similar problems exist in claim 28.

In claim 23, line 2, it is not clear how to define "a last instruction therein" since there may have many last instructions in the memory.

In claim 27, lines 1-2, it is not clear how a trace can include executable instructions. As set forth above, a trace comprises the sequences of executed instructions (see also page 1, lines 16 in the specification), e.g. it comprises the address

data (or pointers) of executed instructions. The address data is not an instruction.

As set forth above, Claims 23, and 41-43 recited indexing means, however, in the specification there's no description about the structure for the indexing means necessary for supporting the claims.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

11. Claims 1-3, and 38-40, as best understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Kaylor (U.S. Patent No. 5,492,276), hereinafter referred to as Kaylor'276.

Referring to claim 1, Kaylor'276 discloses as claimed: apparatus (see Fig. 5), comprising: a memory entry (10, see Fig. 1), storing a trace (the path of the waterway 20, see Figs. 1 and 5) having a multiple-entry (from 25, 26, 27 see Fig. 1, and 52 and 53 see Fig. 4), single exit (79 along the exit axis 23, see Fig. 5) architecture. Note apparatus (see Fig. 5) is best reasonably and broadly interpreted as a memory entry to comprise many water traces. Note claims 38 recites the corresponding limitations as set forth in claim 1 above.

As to claims 2, and 39 Kaylor'276 also discloses: the trace being a complex trace (the path of the waterway 20, see Figs. 1 and 5) having multiple independent prefixes (such as 61, 62 as

shown in Fig. 5) and a common, shared suffix (the race along the exit axis 23 as shown in Fig. 5).

As to claims 3, and 40, Kaylor'276 also discloses: the entry (10, see Fig. 1) is indexed by an address (reasonably and broadly interpreted as a mark, a model NO., or a serial No. of the apparatus 10) of a terminal instruction (reasonably and broadly interpreted such as a user's manual) therein.

12. Claims 1, 2, 16, 20, 28, 29, 38, and 39, as best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Agarwal (U.S. Patent No. 5,966,541), hereinafter referred to as Agarwal'541.

Referring to claim 1, Agarwal'541 discloses as claimed: a memory entry (the memory space containing blocks 101, 102 and 103 as shown in Fig. 8; Note a memory entry is best broadly and reasonable interpreted as a memory space where information can be stored or retrieved since the range or size of a memory entry can be various), storing a trace (an extended block including blocks 101, 102 and 103 as shown in Fig. 8. Note "traces" are also called -extended blocks- see page 2, lines 23-24 in the specification) having a multiple-entry (entry points I3 and I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8)

architecture. Note Fig. 8 is best reasonably and broadly interpreted as to comprise a trace (extended block) comprising block 101 to block 103 as shown in Fig. 8. Note claim 38 recites the corresponding limitations as set forth in the claim 1.

Referring to claim 16, Agarwal'541 discloses as claimed: A processing engine (certainly existing in Agarwal'541's system for processing the instructions therein), comprising: a front end stage (such as the stage before the instructions are fetched in the Agarwal'541's system) to store blocks (in memory 703, see Fig. 11, and Col. 11, line 36), including blocks 101, 102 and 103 as shown in Fig. 8) of instructions in a multiple-entry (I3 and I5, see Fig. 8), single exit (I9 in block 103, see Fig. 8) architecture when considered according to program flow, and an execution unit (certainly existing in Agarwal's system for executing the instructions therein) in communication with the front end stage.

Referring to claim 20, Agarwal'541 discloses as claimed: apparatus, comprising a memory entry storing (in memory 703, see Fig. 11, and Col. 11, line 36) a sequence of program instructions (from I3 to I9 see Fig. 8) as a trace (an extended block including blocks 101, 102 and 103 as shown in Fig. 8. Note "traces" are also called -extended blocks- see page 2, lines 23-24 in the specification), the instructions defining a program

flow that progresses (note Fig. 8 shows the program flow progresses instruction to instruction) from any instruction (instructions from I3 to I8 see Fig. 8. Note broadly, the program flow progresses from different instructions at different time during execution) therein to a last instruction (last instruction I9 see Fig. 8) in the trace and in which the trace has multiple separate prefixes (block 101 and block 102 are the prefixes in the extended block comprising blocks 101, 102, and 103 as shown in Fig. 8).

Referring to claim 28, Agarwal'541 discloses as claimed: a trace (an extended block including blocks 101, 102 and 103 as shown in Fig. 8. Note "traces" are also called -extended blocks- see page 2, lines 23-24 in the specification), comprising a sequence of program instructions (from I3 to I9 see Fig. 8) stored together (in memory 703, see Fig. 11, and col. 11, line 36) assembled in order according to program flow, the sequence having a multiple-entry (entry points I3 and I5, see Fig. 8), single exit (I9 in block 103, see Fig. 8) architecture. Note Fig. 8 is best reasonably and broadly interpreted as to comprise a trace (extended block) comprising block 101 to block 103 as shown in Fig. 8.

Referring to claim 38, Agarwal'541 discloses as claimed: a memory (memory 703, see Fig. 11, and Col. 11, line 36) having at

least one memory entry (the memory space containing blocks 101, 102 and 103 as shown in Fig. 8; Note a memory entry is best broadly and reasonable interpreted as a memory space where information can be stored or retrieved since the range or size of a memory entry can be various). Note that what it is intended "to store" is immaterial. Therefore, the limitation, "a trace having a multiple entry, single exit architecture" does not provide any patentable weight.

As to claims 2, 29 and 39, Agarwal'541 also discloses: the trace being a complex trace (including blocks 101, 102 and 103 as shown in Fig. 8) having multiple independent prefixes (block 101 and block 102 as shown in Fig. 8) and a common, shared suffix (block 103 is the as shown in Fig. 8). Further, in claim 39, "a trace is a complex trace having multiple independent prefixs and a common, shared suffix" to be stored is immaterial and the claim fails to further limit the subject matter from claim 38.

Response to Arguments

13. Appellant's arguments in Appeal Brief and Supplemental Appeal Brief mailed 6/28/05 and 1/13/06 respectively have been

considered but are moot in view of the new explanation and the new ground(s) of rejection.

Regarding 35 U.S.C. §101, and 35 U.S.C. §112, first and second paragraph problems, Applicant's response has not completely overcome these rejections.

Appellants argue that "Agarwal does not mention traces at all. A trace is a specific code structure that occurs in processor. This structure cannot be found in Agarwal." (page 5, lines 16-18 of Appeal Brief). Agarwal does not explicitly mention traces. However, as set forth in claim 1 art rejections, Agarwal'541 discloses as claimed: storing a trace (an extended block including blocks 101, 102 and 103 as shown in Fig. 8. Note "traces" are also called -extended blocks- see page 2, lines 23-24 in the specification) having a multiple-entry (entry points I3 and I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture. Agarwal'541 teaches the claimed invention based on the definition of "traces" particularly specified by Appellant in the specification.

Appellants argue that "concerning claim 1, the Examiner alleges that (1) "it is not clear how a trace can have a multi-entry and a single exit," that (2) "the flow of a program can

only have an (sic; it is assumed "one" is meant) entry in a trace," and that (3) "some more detailed descriptions are missing." See Office Action, page 5, item 6, par. 2. In response to points (1) and (3), it is observed that it is not the role of the claims to describe or explain the invention; that is the role of the written description. As to point (2), the Examiner's statement is palpably inaccurate. Program logic can be designed to have many entry points. A conditional branch is only example of how a program flow can be entered at multiple different points." (page 3, lines 12-20 of Supplemental Appeal Brief).

Examiner disagrees with Appellants. As set forth above, the flow of a program can only have one entry in a trace (see the attached reference of Nair Ravi, " Trace Caches and Trace Processors", lecture note, Pages 1-2, USPTO training for examiners in the computer architecture area, 4/29/04) since the trace is dependent on the input to the program. A trace is not a program. Regarding points (1) and (3), some essential elements or more detailed descriptions are missing in the claim. Note while it is appropriate to use the specification to determine what applicant intends a term to mean, a positive limitation from the specification cannot be read into a claim that does not impose that limitation [see MPEP 2106].

Appellants argue that "Claims 1-3 and 38-40 were rejected under 35 USC 1 102(b) as being anticipated by Kaylor (U.S. 5,492,276) ("Kaylor"). This rejection constitutes unmitigated error... The Kaylor reference, by contrast, relates to plumbing. Not a single element in the Kaylor reference can fairly be found under any reasonable interpretation to correspond to any element of the rejected claims." (page 4, last three lines and page 5, lines 1-6 of Supplemental Appeal Brief). Examiner disagrees with Appellants. A rejection under section 102 is proper by using nonanalogous prior art. See MPEP 2131.05 [R-2].

"Arguments that the alleged anticipatory prior art is nonanalogous art' or teaches away from the invention' or is not recognized as solving the problem solved by the claimed invention, [are] not germane' to a rejection under section 102." Twin Disc, Inc. v. United States, 231 USPQ 417, 424 (Cl. Ct. 1986) (quoting In re Self, 671 F.2d 1344, 213 USPQ 1, 7 (CCPA 1982)). >See also State Contracting & Eng ' g Corp. v. Condotte America, Inc., 346 F.3d 1057, 1068, 68 USPQ2d 1481, 1488 (Fed. Cir. 2003) (The question of whether a reference is analogous art is not relevant to whether that reference anticipates. A reference may be directed to an entirely different problem than the one addressed by the inventor, or may be from an entirely different field of endeavor than that of the claimed invention, yet the reference is still anticipatory if it explicitly or inherently discloses every limitation recited in the claims.).< A reference is no less anticipatory if, after disclosing the invention, the reference then disparages it. The question whether a reference "teaches away" from the invention is inapplicable to an anticipation analysis. Celeritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir. 1998) (The prior art was held to anticipate the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed."). See also Atlas Powder Co. v. IRECO, Inc., 190 F.3d 1342, 1349, 51 USPQ2d 1943, 1948 (Fed. Cir. 1999)(Claimed composition was anticipated by prior art reference that inherently met claim limitation of "sufficient aeration" even though reference taught away from air entrapment or purposeful aeration.) See MPEP 2131.05 [R-2].

Contact Information

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Fritz M. Fleming, can be reached on (571) 272-4145. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

15. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 571-273-8300.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

Supervisory FRITZ FLEMING PRIMARY EXAMINER GROUP 2100 AU 2181 4/3/2006

HENRY W. H. TSAI
PRIMARY EXAMINER
April 3, 2006